Applicant : Keiji Negi   Attorney's Docket No.: 10830-048001 / A36-
Serial No. : 09/723,194   126904M/YAH
Filed : November 27, 2000
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Amendments to the Specification:

Please replace the paragraph beginning at page 9, line 8 with the following amended paragraph:

--Fig. 2 is a truth table showing operation examples of a shift circuit~s~ A to E ~~and sort circuits A to D of the embodiment~~;--

Please replace the paragraph beginning at page 9, line 10 with the following amended paragraph:

--Fig. 3 is a truth table showing operation examples of <u>sort circuits A to C</u> ~~shift circuits B to D of the embodiment~~;--

Please replace the paragraph beginning at page 9, line 12 with the following amended paragraph:

--Fig. 4 is a truth table showing operation examples in an enable state of <u>sort circuits D to F</u> ~~one-bit shift circuits A to C of the embodiment~~;--

Please replace the paragraph beginning at page 13, line 24 with the following amended paragraph:

-- In signals inputted to the second sort part 7, the signals sampled every m bits as BIT 0, BIT m, BIT 2m, ⋯ , BIT (n-1) · m are inputted to the delay circuit 10. Also, signals in which the signals inputted to the delay circuit 10 are shifted by one bit as BIT 1, BIT (m+1), BIT (2m+1), ⋯ , BIT ((N-1) · m+1) are inputted to the next sort circuit 11a. Similarly, ~~signals in which the~~ signals inputted to the sort circuit 11a are shifted by one bit ~~are~~ <u>and</u> inputted to the sort circuit 11b, and ~~signals in which the~~ signals inputted to the sort circuit 11b are further shifted by one bit ~~are~~ <u>and</u> inputted to the sort circuit 11c.--

Amendments to the Claims: